Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A wireless communication device for use in a DS/CDMA mobile communication system, the wireless communication device being operable in response to a sequence of reception signals divisible into a plurality of frames each of which has a frame rate and which is further divided into a plurality of slots, the reception signal sequence being processed with a processing time and a delay time in the wireless communication device, comprising:

processing means for statistically processing preceding frame rates in previously received ones of the frames to produce a result of statistical processing, the previously received frames being determined on the basis of a time difference between the processing time and the delay time;

predicting means for predicting a later one of the frame rates in a next one of the frames on the basis of the result of statistical processing to produce a predicted frame rate of the later one of the frame, the next frame being determined with reference to the time difference between the processing time and the delay time; and

executing means for executing a predetermined operation within candidate ones of the slots determined for the predicted frame rate.

2. (Original) A wireless communication device as claimed in claim 1, wherein the result of statistical processing is successively renewed so as to be matched with a variation of environment.

3. (Original) A wireless communication device as clammed in claim 1, wherein the executing means comprises:

a spread code generator for generating a spread code; and

a calculating unit for calculating the candidate slots from the predicted frame rate and the spread code.

4. (Original) A wireless communication device as claimed in claim 3, wherein the executing means further comprises:

a demodulating unit for demodulating the reception signal with reference to the candidate slots into a demodulated signal.

5. (Currently Amended) A method ~~of~~ for use in a wireless communication device to ~~predicting~~ predict a frame rate in a selected one of frames that follows a reference frame with a reference frame rate, comprising the steps of:

statistically processing the reference frame rate and a previous frame rate of a previous frame preceding the reference frame to calculate a frame rate candidate in the selected one of the frames, the preceding frame being determined on the basis of a delay time which is needed in the wireless communication device; and

producing the frame rate candidate as the frame rate predicted.

6 (Original) A method as claimed in claim 5, wherein the statistically processing step comprises:

successively storing the previous and the reference frame rates;

accumulating each combination of the previous and the reference frame rates to statistically detect a frequency of each combination; and

obtaining the frame rate candidate by using the frequency of each combination.

7. (Currently Amended) A circuit operable in response to a sequence of frame rate signals derived from a sequence of reception signals in a wireless communication device of a mobile communication system, the reception signal sequence being processed with a processing time and a delay time in the wireless communication device and including a reference frame, a previous frame sequence preceding the reference frame, and a later frame following the reference frame while the circuit is used for calculating a later frame rate of the later frame, comprising:

processing means for statistically processing a reference frame rate extracted from the reference frame and a previous frame rate extracted from the preceding frame sequence selected with reference to a time difference between the processing time and the delay time to

successively store a frame rate candidate in the later frame as a result of statistically processing; and

selecting means for selecting the frame rate candidate from the later frame determined with reference to the time difference to produce the frame rate candidate as the later frame rate.

8. (Currently Amended) A circuit as claimed in claim 7, the wireless communication device having a processing time for decoding the reception signal sequence into a sequence of reception signals, wherein the ~~producing~~ processing means comprises:

an input register which has a plurality of stages successively loaded with each frame rate extracted from the reception signal sequence at each frame;

a frequency storage section, coupled to a plurality of the stages of the input register dependent on the processing time, for successively storing a combination of the frame rate given from the reference and the previous frame rates;

a candidate calculator for calculating the frame rate candidate of the later frame by statistically detecting frequencies of each combination; and

a candidate register for successively registering the frame rate candidate of the later frame.

9. (Original) A circuit as claimed in claim 8, wherein the selecting means comprises:

a later frame selector, coupled to the stages of the input register that are dependent on the processing time, for selecting the frame rate candidate by a combination of the frame rates derived from the stages of the input register.

10. (Currently Amended) A circuit as claimed in ~~claim 7~~claim 8, the wireless communication device being also operable in response to a delayed signal which is delayed by a delay time relative to the reception signal sequence, wherein the frequency storage section is coupled to the plurality of the stages of the input register that are determined by a difference between the processing time and the delay time.

11. (Currently Amended) A circuit as claimed in ~~claim 10~~claim 9, wherein the later frame selector is coupled to the plurality of the stages of the input register that are also determined by the difference between the processing time and the delay time.

12. (Currently Amended) A circuit as claimed in ~~claim 10~~claim 8, wherein the plurality of the stages of the input register to which the frequency storage section is coupled are defined as a first relationship in consideration of the difference between the processing and the delay times while a relationship among the frame rate candidate stored in the candidate register and the stages of the input register to which the later frame selector is coupled is specified by a second relationship similar to the first relationship.

13. (Original) A circuit as claimed in claim 10, wherein the difference between the processing and the delay times is not greater than a time duration of three frames.

14. (Original) A circuit as claimed in claim 13, wherein each of the current, the previous, and the later frame rates is selected from four different frame rates.

15. (Currently Amended) A circuit as claimed in ~~claim 14~~claim 8, wherein the frequency storage section has a plurality of frequency registers which are determined in number by the four frame rates and the number of the stages of the input register to which the frequency storage section is coupled..

16. (Currently Amended) A circuit as claimed in claim 15, wherein the frequency registers are equal in number to sixty-four when the number of the stages of the input register is equal to three.

17. (Original) A circuit as claimed in claim 15, wherein each of the frequency registers has first through y-th memory cells, where y is an integer.

18. (Cancelled).

19. (Currently Amended) A method of predicting a latest frame rate of a latest received frame from preceding frame rates, comprising the steps of:

extracting a sequence of frame rate signals from a sequence of reception signals; and

predicting the latest frame rate of the latest received frame by processing previous ones of the frame rate signals preceding the latest received frame in consideration of a delay time for extracting the frame rate signal sequence~~A method as claimed in claim 18~~, used for controlling a searcher included in a wireless communication device of a CDMA communication system, further comprising the step of:

supplying the latest and predicted frame rate through a data burst randomizer to the searcher.

20. (Original) A method as claimed in claim 19, wherein the delay time is determined by a difference between a processing time in the wireless communication device and an additional delay time given a delay unit which delays the reception signal sequence.

21. (Original) A method as claimed in claim 20, wherein the predicting step comprises the steps of:

successively registering the frame rate signals in an input register;

detecting a combination of the frame rate signals from the registered frame rate signals by selecting stages of the input register in consideration of the delay time to store a frequency of each, combination;

calculating a later frame rate candidate from the frequencies of the combinations; and

selecting the later frame rate from the later frame rate candidate in consideration of the delay time.

22. (Original) A method as claimed in claim 20, wherein the stages of the input register selected at the detecting step provide a first relationship while the later frame rate is selected by using a second relationship similar to the first relationship.